

Abstract of the Disclosure

A carry look-ahead adder may include: a carry generation circuit to generate carry propagation bit values and carry kill bit values for M blocks based on an N-bit addend and augend; a block carry circuit to generate block carry signals based upon the bit values; a Manchester-carry-chain configured bit carry circuit to generate first bit carry signals where a block carry exists in each of the M blocks and second carry bit signals where no block carry exists, based on the bit values; a control circuit to generate, independently of a clock enable signal at a logical level, selection-control signals based upon the block carry signals; and a summation selection circuit to select between the first bit carry signals and the second bit carry signals and to add the carry propagation bit values and the selected carry signals.